

## **AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

### **Listing of Claims:**

1           1. (Original) A method for supporting directory-based cache coherence in  
2     an object-addressed memory hierarchy in a computer system, comprising:  
3           receiving a cache-coherence transaction for a cache line;  
4           if the cache line is an object-addressed cache line, using a corresponding  
5     object identifier and offset to look up directory information specifying where  
6     copies of the object-addressed cache line are located in the caches in the computer  
7     system; and  
8           using the directory information to perform the cache-coherence  
9     transaction.

1           2. (Original) The method of claim 1, wherein if the cache line is a  
2     physically-addressed cache line, the method further comprises using a  
3     corresponding physical address to look up directory information specifying where  
4     copies of the physically-addressed cache line are located in the caches.

1           3. (Original) The method of claim 1, wherein the method is performed by a  
2     memory controller that resides between main memory and caches in the computer  
3     system.

1           4. (Original) The method of claim 1, wherein looking up the directory  
2     information involves looking up the directory information in main memory.

1           5. (Original) The method of claim 1,  
2           wherein directory information for a physically-addressed cache line is  
3           located alongside a corresponding physical cache line in main memory; and  
4           wherein directory information for multiple object-addressed cache lines  
5           can be stored in a single physical cache line in main memory.

1           6. (Original) The method of claim 1, wherein when directory information  
2           for a given cache line is replaced by directory information for another cache line  
3           or is otherwise removed, the method further comprises flushing and/or  
4           invalidating any copies of the given cache line that are located in caches in the  
5           computer system.

1           7. (Original) The method of claim 1, wherein using the corresponding  
2           object identifier and offset to look up the directory information in memory  
3           involves performing a hash lookup.

1           8. (Original) The method of claim 1, wherein the memory controller  
2           includes a translator that translates between object identifiers (used to reference  
3           objects in an object cache) and physical addresses (used to address objects in main  
4           memory).

1           9. (Original) The method of claim 8,  
2           wherein prior to receiving a request to access an object at the translator,  
3           the request is initially directed to the object cache;  
4           wherein if the request causes a hit in the object cache, the object is  
5           accessed in the object cache and the request is not sent to the translator; and  
6           wherein if the request causes a miss in the object cache, the request is sent  
7           to the translator.

1           10. (Original) The method of claim 1, wherein the cache-coherence  
2 transaction can involve:  
3           a store to the cache line;  
4           a load from the cache line;  
5           an invalidation of the cache line; or  
6           any other change in a cache-coherence-related state of the cache line.

1           11. (Original) The method of claim 1, wherein the caches include one or  
2 more levels of caches.

1           12. (Original) The method of claim 1, wherein object-addressed cache  
2 lines are used to store objects defined within an object-oriented programming  
3 system.

1           13. (Original) An apparatus that supports directory-based cache coherence  
2 in an object-addressed memory hierarchy in a computer system, comprising:  
3           a receiving mechanism configured to receive a cache-coherence  
4 transaction for a cache line;  
5           a lookup mechanism, wherein if the cache line is an object-addressed  
6 cache line, the lookup mechanism is configured to use a corresponding object  
7 identifier and offset to look up directory information specifying where copies of  
8 the object-addressed cache line are located in the caches; and  
9           a cache-coherence mechanism configured to use the directory information  
10 to perform the cache-coherence transaction.

1           14. (Original) The apparatus of claim 13, wherein if the cache line is a  
2 physically-addressed cache line, the lookup mechanism is configured to use a

3 corresponding physical address to look up directory information specifying where  
4 copies of the physically-addressed cache line are located in the caches.

1 15. (Original) The apparatus of claim 13, wherein the receiving  
2 mechanism, the lookup mechanism and the cache coherence mechanism are  
3 located within a memory controller that resides between main memory and caches  
4 in the computer system.

1 16. (Original) The apparatus of claim 13, wherein the lookup mechanism  
2 is configured to look up the directory information in main memory.

1 17. (Original) The apparatus of claim 13,  
2 wherein directory information for a physically-addressed cache line is  
3 located alongside a corresponding physical cache line in main memory; and  
4 wherein directory information for multiple object-addressed cache lines  
5 can be stored in a single physical cache line in main memory.

1 18. (Original) The apparatus of claim 13, further comprising an  
2 invalidation mechanism, wherein when directory information for a given cache  
3 line is replaced by directory information for another cache line or is otherwise  
4 removed, the invalidation mechanism is configured to flush and/or invalidate any  
5 copies of the given cache line that are located in caches in the computer system.

1 19. (Original) The apparatus of claim 13, wherein the lookup mechanism  
2 is configured to use the corresponding object identifier and offset to perform a  
3 hash lookup to obtain the directory information.

1           20. (Original) The apparatus of claim 13, wherein the memory controller  
2 includes a translator that translates between object identifiers (used to reference  
3 objects in an object cache) and physical addresses (used to address objects in main  
4 memory).

1           21. (Original) The apparatus of claim 20, further comprising an object  
2 cache;  
3           wherein the request is initially directed to the object cache;  
4           wherein if the request causes a hit in the object cache, the apparatus is  
5 configured to access the object in the object cache and is configured not to send  
6 the request to the translator; and  
7           wherein if the request causes a miss in the object cache, the apparatus is  
8 configured to send the request to the translator.

1           22. (Original) The apparatus of claim 13, wherein the cache-coherence  
2 transaction can involve:  
3           a store to the cache line;  
4           a load from the cache line;  
5           an invalidation of the cache line; or  
6           any other change in a cache-coherence-related state of the cache line.

1           23. (Original) The apparatus of claim 13, wherein the caches include one  
2 or more levels of caches.

1           24. (Original) The apparatus of claim 13, wherein object-addressed cache  
2 lines are used to store objects defined within an object-oriented programming  
3 system.

1           25. (Original) A computer system that supports directory-based cache  
2 coherence in an object-addressed memory hierarchy, comprising:  
3           one or more processors;  
4           a set of caches coupled to the one or more processors;  
5           a main memory;  
6           a memory controller that couples together the set of caches and the main  
7 memory;  
8           a receiving mechanism within the memory controller configured to receive  
9 a cache-coherence transaction for a cache line;  
10          a lookup mechanism within the memory controller,  
11                wherein if the cache line is an object-addressed cache line,  
12                the lookup mechanism is configured to use a corresponding object  
13                identifier and offset to look up directory information specifying  
14                where copies of the object-addressed cache line are located in the  
15                caches, and  
16                wherein if the cache line is a physically-addressed cache  
17                line, the lookup mechanism is configured to use a corresponding  
18                physical address to look up directory information specifying where  
19                copies of the physically-addressed cache line are located in the  
20                caches; and  
21          a cache-coherence mechanism configured to use the directory information  
22 to perform the cache-coherence transaction.